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COMMODORE 64 TECHNICAL OVERVIEW

EATURES

6510 MICROPROCESSOR: 6502 COMPATIBLE

6566 VIDEO DISPLAY CHIP:
* 40 COLUMN BY 25 LINE CHARACTER DISPLAY WITH INDEPENDENT FOREGROUND AND BACKGROUND COLORS
* USER PROGRAMMABLE CHARACTERS
* 320 X 200 PIXEL COLOR BIT-MAP, 2 COLORS PER 8 X 8 PIXEL ZONE
* 160 X 200 PIXEL 'MULTI-COLOR' BIT-MAP, 4 COLORS PER 8 X 4 PIXEL ZONE
* 16 COLORS AVAILABLE SIMULTANEOUSLY
* 256 INDEPENDENTLY MOVEABLE DISPLAY OBJECTS WITH UP TO 8 PER LINE
  - EACH OBJECT IS 24 X 21 PIXELS
  - COLLISION DETECTION BETWEEN OBJECTS
  - SELECTABLE OBJECT DISPLAY PRIORITY
  - MULTICOLOR OBJECTS
* HORIZONTAL OR VERTICAL SCROLLING BY PIXEL

6581 SID SOUND SYNTHESIZER CHIP
* 3 INDEPENDENT VOICES, EACH WITH:
  - 9 OCTAVE RANGE (.059Hz-3.9KHz in .059Hz steps)
  - 4 WAVEFORMS: SAWTOOTH, TRIANGLE, VARIABLE PULSE, AND NOISE
  - AMPLITUDE MODULATION
  - PROGRAMMABLE ADSR ENVELOPE GENERATOR
  - RING MODULATION
  - OSCILLATOR SYNCHRONIZATION
* PROGRAMMABLE FILTER
  - INDEPENDENTLY SELECTABLE FOR EACH VOICE
  - LOW PASS, HIGH PASS, BAND PASS, AND NOTCH OUTPUTS
  - VARIABLE RESONANCE
* MASTER VOLUME CONTROL

)ESIGN FEATURES:

KEYBOARD:
- 64 KEY FULL-STROKE
- CHARACTER COLORS SELECTABLE DIRECTLY FROM KEYBOARD

GAME CONTROLLERS:
- JOYSTICKS
- PADDLES
- LIGHT PEN

PLUG-IN CARTRIDGE:
- COMPATIBLE WITH COMMODORE ULTIMAX CARTRIDGES

/O SYSTEMS:
- 8 BIT USER PORT
- CBM SERIAL BUS
- CBM CASSETTE INTERFACE
- 44 PIN EXPANSION BUS/CARTRIDGE SLOT
- RF MODULATOR WITH SOUND FOR TV HOOKUP
- 75 OHM COMPOSITE VIDEO OUTPUT FOR MONITOR
- AUDIO OUTPUT FROM SYNTHESIZER

EMORY CONFIGURATION:
- 1K SCREEN RAM
- 1K COLOR RAM-NIBBLES
- 52K MACHINE LANGUAGE USER RAM
  (38K BASIC USER RAM)
- 8K BASIC ROM
- 8K KERNAL ROM
- 4K CHARACTER ROM

CCESSORIES:
- PLUG-IN GAME AND APPLICATION CARTRIDGES
- SINGLE DISK DRIVE (170K)
- TRACTOR FEED IMPACT GRAPHICS PRINTER
- DIRECT CONNECT MODEM
- RS-232 CARTRIDGE
- IEEE CARTRIDGE
- JOYSTICKS
- PADDLES
- LIGHT PEN
- CASSETTE UNIT

UTURE ACCESSORIES:
- Z-80 MICROROCESSOR CARD
- SOFT LOADED LANGUAGES:
  * CBM BASIC 4.0
  * UCSD PASCAL
- SUPPORT FOR:
  * FORTH
  * PILOT

- EXTENDED BASIC ROM CARTRIDGE
  * BASIC GRAPHIC COMMANDS
  * BASIC SOUND/MUSIC COMMANDS

- PROGRAMMER'S AID CARTRIDGE
  * ENHANCED EDITOR
  * PROGRAM TRACE
  * RENUMBER

- EXTENDED MACHINE LANGUAGE MONITOR ROM CARTRIDGE
  * MONITOR
  * DEBUGGER
  * ASSEMBLER
  * DISASSEMBLER

COMMODORE ULTIMAX TECHNICAL OVERVIEW

EATURES

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* 320 X 200 PIXEL RESOLUTION
* 16 COLORS AVAILABLE SIMULTANEOUSLY
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  - EACH OBJECT IS 24 X 21 PIXELS
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6581 SID SOUND SYNTHESIZER CHIP
* 3 INDEPENDENT VOICES, EACH WITH:
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  - 4 WAVEFORMS: SAWTOOTH, TRIANGLE, VARIABLE PULSE, AND NOISE
  - AMPLITUDE MODULATION
  - PROGRAMMABLE ADSR ENVELOPE GENERATOR
  - RING MODULATION
  - OSCILLATOR SYNCHRONIZATION
* PROGRAMMABLE FILTER
  - INDEPENDENTLY SELECTABLE FOR EACH VOICE
  - LOW PASS, HIGH PASS, BAND PASS, AND NOTCH OUTPUTS
  - VARIABLE RESONANCE
* MASTER VOLUME CONTROL

)ESIGN FEATURES:

:EYBOARD:
- FLAT MEMBRANE KEYBOARD

;AME CONTROLLERS:
- JOYSTICKS
- PADDLES
- LIGHT PEN

'LUG-IN CARTRIDGE:
- COMPATIBLE WITH COMMODORE 64 GAME CARTRIDGES

:/O SYSTEMS:
- CBM CASSETTE INTERFACE
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- 75 OHM COMPOSITE VIDEO OUTPUT FOR MONITOR
- AUDIO OUTPUT FROM SYNTHESIZER

1EMORY CONFIGURATION:
- 1K SCREEN RAM
- 1K COLOR RAM-NIBBLES

CCESSORIES:

- BASIC LANGUAGE CARTRIDGE
- PLUG-IN GAME AND APPLICATION CARTRIDGES
- JOYSTICKS
- PADDLES
- LIGHT PEN
- CASSETTE UNIT

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OMMODORE 64 MEMORY MAP

OCATION			DESCRIPTION
HEX	DECIMAL		
000-03FF	0-1023		ZERO PAGE BASIC POINTERS/STACK/ETC.
400-07FF	1024-2047		SCREEN RAM
800-9FF	2048-40959		PROGRAM TEXT AREA
000-9FFF	32768-40959		8K CARTRIDGE ROM AREA
000-BFFF	40960-53247		8K BASIC (V2)
000-CFFF	53248-57343		4K RAM
000-DFFF	57344-58367		'66-'81-'26(2)-IO EXP1&2/4K CHAR SPACE
000-D3FF	57344-58367		6566 VIDEO CHIP
000	57344		SPRITE 0 X CMP
001	57345		SPRITE 0 Y CMP
002	57346		SPRITE 1 X CMP
003	57347		SPRITE 1 Y CMP
004	57348		SPRITE 2 X CMP
005	57349		SPRITE 2 Y CMP
006	57350		SPRITE 3 X CMP
007	57351		SPRITE 3 Y CMP
00[illegible]	57352		SPRITE 4 X CMP
009	57353		SPRITE 4 Y CMP
00A	57354		SPRITE 5 X CMP
00B	57355		SPRITE 5 Y CMP
00C	57356		SPRITE 6 X CMP
00D	57357		SPRITE 6 Y CMP
00E	57358		SPRITE 7 X CMP
00F	57359		SPRITE 7 Y CMP
010	57360		SPRITE X CMP (MSB OF X COORD.)
011	57361	BIT 7	RASTER COMPARE
		BIT 6	EXTENDED COLOR MODE
		BIT 5	BIT MAP MODE
		BIT 4	UNUSED
		BIT 3	24/25 ROW SELECT (1=25 ROWS)
		BIT 2-0	SCROLL IN Y POSITION
012 (R/O)			RASTER READ (RASTER CMP IRQ WRITE)
013 (R/O)	57362		LIGHT PEN LATCH X
014 (R/O)	57363		LIGHT PEN LATCH Y
015	57364		SPRITE DISABLE (1=SPRITE ENABLED)
016	57365	BIT 7-5	UNUSED
		BIT 4	MULTI-COLOR MODE
		BIT 3	38/40 COLUMN SELECT (1=40 COL.)
		BIT 2-0	SCROLL IN X POSITION
017	57366		SPRITE EXPAND IN "Y"
01[illegible]	57367	BIT 7-4	VIDEO MATRIX BASE
		BIT 3-1	CHARACTER SPACE BASE
019	57368	BIT 7	FOLLOWS IRQ LINE
		BIT 2	IRQ FOR SPRITE TO SPRITE COLLISION
		BIT 1	IRQ FOR SPRITE TO BACKGROUND COLLISION
		BIT 0	RASTER CMP IRQ

01A	57369	IRQ MASK REGISTER (0= INTERRUPT DISABLED)
01B	57370	BACKGROUND TO SPRITE PRIORITY
01C	57371	MULTI-COLOR SPRITE SELECT
01D	57372	SPRITE EXPAND IN "X"
01E	57373	SPRITE TO SPRITE COLLISION DETECT
01F	57374	SPRITE TO BACKGROUND COLLISION DETECT
	COLOR REGISTERS (BIT 3-0)	
020	57375	BORDER COLOR
021	57376	BACKGROUND COLOR 0
022	57377	BACKGROUND COLOR 1
023	57378	BACKGROUND COLOR 2
024	57379	BACKGROUND COLOR 3
025	57380	SPRITE MULTI-COLOR REGISTER 0
026	57381	SPRITE MULTI-COLOR REGISTER 1
027	57382	SPRITE 0 COLOR
028	57383	SPRITE 1 COLOR
029	57384	SPRITE 2 COLOR
02A	57385	SPRITE 3 COLOR
02B	57386	SPRITE 4 COLOR
02C	57387	SPRITE 5 COLOR
02D	57388	SPRITE 6 COLOR
02E	57388	SPRITE 6 COLOR

```
400-D7FF                        6581 (SID) SYNTHESIZER CHIP
400                             FREQUENCY LO
401                             FREQUENCY HI
402                             PULSE WIDTH LO
403                 BIT 7-4     UNUSED
                    BIT 3-0     PULSE WIDTH HI
404                 CONTROL REGISTER VOICE 1
                    BIT 7       NOISE
                    BIT 6       PULSE
                    BIT 5       SAWTOOTH
                    BIT 4       TRIANGLE
                    BIT 3       TEST BIT
                    BIT 2       RING MOD
                    BIT 1       SYNC
                    BIT 0       GATE
405                             ATTACK/DECAY REGISTER
406                             SUSTAIN/RELEASE REGISTER
407-D40D            CONTROL REGISTER VOICE 2
          (FUNCTIONALLY IDENTICAL TO D400-D406)
40E-D414            CONTROL REGISTER VOICE 3
          (FUNCTIONALLY IDENTICAL TO D400-D406)
415                             CUTOFF FREQUENCY LO
416                             CUTOFF FREQUENCY HI
41                  BIT 7-4     RESONANCE OF FILTER
                   (BIT 3-0     SELECT SIGNALS TO BE ROUTED THROUGH FILTER BITS
ET TO ZERO APPEAR DIRECTLY AT AUDIO OUTPUT, BITS SET TO 1 WILL BE PROCESSED
HROUGH FILTER)
                    BIT 3       EXTERNAL INPUT
                    BIT 2       VOICE 3
                    BIT 1       VOICE 2
                    BIT 0       VOICE 1
418                (BIT 7-4     SELECT FILTER MODE AND OUTPUT OPTIONS)
                    BIT 7       OFF
                    BIT 6       HIGH PASS
                    BIT 5       BAND PASS
                    BIT 4       LOW PASS
                    BIT 3-0     OUTPUT VOLUME
419                             POT X
41A                             POTY
41B                             OSCILLATOR 3/RANDOM NUMBER GENERATOR
41C                             ENVELOPE 3

800-DBFF                   1K   COLOR NIBBLE
C00-DCFF                        6526 #1 (CIA) I/O CHIP
D00-DDFF                        6526 #2 (CIA) I/O CHIP
E00-DEFF                        I/O EXPANSION #1
F00-DFFF                        I/O EXPANSION #2
E0-FFFF                    8K   KERNAL
```

SER CALLABLE KERNAL ROUTINES

AME	ADDRESS	FUNCTION
CPTR	FFA5	INPUT BYTE FROM SERIAL PORT
HKIN	FFC6	OPEN CHANNEL FOR INPUT
HKOUT	FFC9	OPEN CHANNEL FOR OUTPUT
HRIN	FFCF	INPUT CHARACTER FROM CHANNEL
HROUT	FFD2	OUTPUT CHARACTER TO CHANNEL
IOUT	FFA8	OUTPUT BYTE TO SERIAL PORT
LALL	FFE7	CLOSE ALL CHANNELS AND FILES
LOSE	FFC3	CLOSE A SPECIFIED LOGICAL FILE
LRCHN	FFCC	CLOSE INPUT AND OUTPUT CHANNELS
ETIN	FFE8	GET CHARACTER FROM KEYBOARD BUFFER
OBASE	FFF3	RETURN BASE ADDRESS OF I/O DEVICES
ISTEN	FFB1	COMMAND DEVICE ON THE SERIAL BUS TO LISTEN
OAD	FFD5	LOAD RAM FROM A DEVICE
EMBOT	FF9C	READ/SET BOTTOM OF MEMORY
EMTOP	FF99	READ/SET TOP OF MEMORY
PEN	FFC0	OPEN A LOGICAL FILE
LOT	FFF0	READ/SET X,Y CURSOR POSITION
DTIM	FFDE	READ REAL TIME CLOCK
E T	FFB7	READ I/O STATUS WORD
ES OR	FF87	RESTORE DEFAULT I/O VECTORS
AVE	FFD8	SAVE RAM TO DEVICE
CNKEY	FF9F	SCAN KEYBOARD
CREEN	FFED	RETURN X,Y ORGANIZATION OF SCREEN
ECOND	FF93	SEND SECONDARY ADDRESS AFTER LISTEN
ETLFS	FFBA	SET LOGICAL FIRST AND SECOND ADDRESSES
ETMSG	FF90	CONTROL KERNAL MESSAGES
ETNAM	FFBD	SET FILE NAME
ETTIM	FFDB	SET REAL TIME CLOCK
ETTMO	FFA2	SET TIMEOUT ON SERIAL BUS
TOP	FFE1	SCAN STOP KEY
ALK	FFB4	COMMAND SERIAL BUS DEVICE TO TALK
KSA	FF96	SEND SECONDARY ADDRESS AFTER TALK
DTIM	FFEA	INCREMENT REAL TIME CLOCK
NLSN	FFAE	COMMAND SERIAL BUS TO UNLISTEN
NTLK	FFAB	COMMAND SERIAL BUS TO UNTALK
ECTOR	FF84	READ/SET VECTORED I/O

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OMMODORE ULTIMAX MEMORY MAP

OCATION	DESCRIPTION
0000-07FF	2K RAM (2K)
(0400)	SCREEN
0800-0FFF	2K EXPANSION RAM (2K)
1000-13FF	6566 VIDEO CHIP
1400-17FF	6581 (SID) SYNTHESIZER CHIP
1800-1BFF	1K COLOR NIBBLE
1C00-1FFF	6526 (CIA) I/O CHIP
2000-3FFF	8K CARTRIDGE ROM AREA

REGISTER DESCRIPTION FOR THE 6566 VIDEO CHIP
AS USED IN THE COMMODORE 64:

EGISTERS 0-15 ARE PAIRED LIKE 0 AND 1 FOR SPRITES 0-7.

EGISTERS 0-1 CONTROL THE COORDINATE POSITION OF SPRITE ZERO; REGISTER 0 ONTROLS X AXIS AND REGISTER 1 CONTROLS Y AXIS.

EGISTERS 16 IS THE MOST SIGNIFICANT BIT OF THE X COORDINATE OF THE SPRITES, HIS WAY WE CAN MOVE A SPRITE ALL THE WAY ACROSS THE 320 PIXEL X AXIS. BIT 0 ORRESPONDS TO SPRITE ZERO AND SO ON.

EGISTER 17 IS A MULTIFUNCTION REGISTER:
- BIT 0-2 SCROLL IN Y POSITION
- BIT 3 24/25 ROW SELECT (1=25 ROWS)
- BIT 4 NOT USED
- BIT 5 BIT MAP MODE
- BIT 6 EXTENDED COLOR MODE
- BIT 7 RASTER COMPARE

EGISTER 18 IS THE RASTER COMPARE IRQ WRITE REGISTER AND IS READ ONLY.

EGISTERS 19 AND 20 ARE LIGHT PEN LATCHES FOR X AND Y AND ARE READ ONLY.

EGISTER 21 IS THE SPRITE ENABLE REGISTER, EACH BIT SET (0-7) CORRESPONDS TO A PRITE (0-7).

EGISTER 22 IS ANOTHER MULTIFUNCTION REGISTER:
- BIT 0-2 SCROLL IN X POSITION
- BIT 3 38/40 COLUMN SELECT (1=40 COLUMNS)
- BIT 4 MULTI COLOR MODE
- BIT 5-7 NOT USED

EGISTER 23 IS THE SPRITE EXPAND IN Y REGISTER, SETTING THE BIT CORRESPONDING TO SPRITE DOUBLES THE VERTICAL SIZE (Y) OF THE SPRITE.

EGISTER 24 IS A DUAL FUNCTION REGISTER:
- BIT 0 UNSUED
- BIT 1-3 CHARACTER SPACE BASE
- BIT 4-7 VIDEO MATRIX BASE

EGISTER 25 IS IRQ REGISTER:
- BIT 0 RASTER CMP IRQ
- BIT 1 IRQ FOR SPRITE-BACKGROUND COLLISION
- BIT 2 IRQ FOR SPRITE-SPRITE COLLISION
- BIT 3 LIGHT PEN IRQ
- BIT 4-7 NOT USED

EGISTER 26 IS IRQ MASK REGISTER: (0=INTERRUPT DISABLED).

EGISTER 27 IS BACKGROUND-SPRITE PRIORITY REGISTER (0=SPRITE HAS PRIORITY).

EGISTER 28 IS THE MULTICOLOR SPRITE SELECT.

EGISTER 29 IS THE SPRITE EXPAND IN X REGISTER (SEE REGISTER 23).

EGISTER 30 IS THE SPRITE-SPRITE COLLISION DETECTION REGISTER.

EGISTER 31 IS THE SPRITE-BACKGROUD COLLISION DETECTION REGISTER.

EGISTERS 32-46 ARE 4 BIT COLOR REGISTERS:

OLOR CODES

VALUE	COLOR
0	BLACK
1	WHITE
2	RED
3	CYAN
4	PURPLE
5	GREEN
6	BLUE
7	YELLOW
8	ORANGE
9	BROWN
10	LT RED
11	GRAY 1
12	GRAY 2
13	LT GREEN
14	LT BLUE
15	GRAY 3

EGISTER	FUNCTION
32	EXTERIOR COLOR
33	BACKGROUND 0
34	BACKGROUND 1
35	BACKGROUND 2
36	BACKGROUND 3
37	SPRITE multicolor reg 0
38	SPRITE multicolor reg 1
39	SPRITE 0 color
40	SPRITE 1 color
41	SPRITE 2 color
42	SPRITE 3 color
43	SPRITE 4 color
44	SPRITE 5 color
45	SPRITE 6 color
46	SPRITE 7 color

1AKING SPRITES IN BASIC ON THE COMMODORE 64:

;PRITE GRAPHICS ARE AN EXCITING FEATURE OF OUR NEW 6566 VIDEO CHIP, THEY ALLOW)S TO DEFINE A 24X21 PIXEL SHAPE IN ONE OF 8 PRIORITY LEVELS AND MOVE IT BY ;IMPLY UPDATING X AND Y COORDINATES WHILE THE CHIP DETECTS COLLISIONS.

:HE SPRITE IS DEFINED BY 63 BYTES OF DATA (21 ROWS OF 3 BYTES) THE SPRITE DATA 'OINTER IS LOCATED IN THE END OF THE 1K OF SCREEN RAM 2040-2047 FOR (SPRITES)-7)INTO THESE POINTERS WE PUT A VALUE CORRESPONDING TO WHICH 64 BYTE BLOCK TO ;ET OUR DATA FROM.

/IDEO CHIP BEGINS AT 13*4096 DECIMAL ($D000 HEX)
.ET'S CALL THIS VALUE "V"

;PRITE ENABLE BYTE IS V+21: SET BITS 0-7 CORRESPONDING TO SPRITE 0-7

:HE X AND Y COORDINATE REGISTERS ARE PAIRED X,Y FOR SPRITES 0-7 IN REGISTERS V+0 :O V+15.

EXAMPLE:

3Y POKING 2042,2 SPRITE 2 WILL GET ITS DATA FROM THE 64 BYTE BLOCK BEGINNING AT :2) 64.

3Y POKING V+21,4 WE WILL ENABLE SPRITE 2 BY SETTING BIT 2.

NOW WE CAN INCREMENT V+4 (X COORD. OF SPRITE 2) AND V+5 (Y COORD. OF SPRITE 2) TO MOVE OUR SPRITE. THE ORIGIN IN ANY CASE IS IN THE UPPER LEFT.

3Y EXPERIMENTING WITH FOR NEXT LOOPS TO MOVE THIS SPRITE YOU MAY NOTICE THAT YOU CANNOT MOVE ALL THE WAY ACROSS THE SCREEN. THIS IS OF COURSE DUE THE FACT THAT THE SCREEN IS 320 PIXELS ACROSS AND OUR X COORD. BYTE CAN ONLY HOLD 255, FORTUNATELY WE CAN SET A MOST SIGNIFICANT BIT OF THE X COORD. IN REGISTER V+16 (3Y SETTING THE BIT CORRESPONDING TO THE SPRITE) AND BEGIN INCREMENTING AGAIN WHEN WE REACH X COORD. 255.

REGISTER DESCRIPTION FOR THE 6581 (SID) SYNTHESIZER AS USED IN THE COMMODORE 64:

THE SID CHIP IS A THREE VOICE POLYPHONIC SYNTHESIZER ON A SINGLE 24 PIN IC. N ADDITION INDEPENDENT ADSR ENVELOPES FOR EACH VOICE THE SID ALLOWS OSC SYNC, ING MOD, HIGH, LOW ,AND BAND PASS FILTERING AS WELL AS TWO A/D CONVERTERS.

EGISTERS 0-6 CONTROL VOICE 1, 7-13 AND 14-20 ARE ORGANIZED SIMILARLY FOR VOICES AND 3 RESPECTIVELY.
EGISTERS 0 AND 1 (S+0,S+1) REPRESENT THE 16 BIT NUMBER WHICH LINEARLY CONTROLS HE FREQUENCY OF OSC 1.
EGISTER 2 (S+2) AND BITS 0-3 OF REGISTER 3 (S+3) REPRESENT THE 12 BIT NUMBER HICH CONTROLS THE PULSE WIDTH OF OSC 1.
EGISTER 4 (S+4) IS THE CONTROL REGISTER FOR OSC 1, IT'S BITS SELECT VARIOUS UTPUT OPTIONS.

BIT 0 GATE BIT: WHEN SET THE ENVELOPE IS TRIGGERED AND TTACK/DEACAY/SUSTAIN CYCLE BEGINS, WHEN UNSET THE RELEASE CYCLE BEGINS.

BIT 1 SYNC BIT: SYNCHRONIZES OSC 1 TO OSC 3.(2 TO 1 FOR VOICE 2, 3 TO 2 OR VOICE 3)

BIT 2 RING MOD BIT: REPLACES OSC 1 OUTPUT WITH THE RING MODULATED UTPUTOF OSC 1 AND OSC 3.(2 AND 1 FOR VOICE 2, 3 AND 2 FOR VOICE 3)

BIT 3 TEST BIT: WHEN SET OSC 1 IS RESET AND LOCKED TO ZERO UNTIL IT IS NSET.

BIT 4 TRIANGLE WAVEFORM: WHEN SET THE TRIANGLE WAVEFORM OUTPUT IS ELECTED. THE TRIANGLE WAVEFORM IS LOW IN HARMONICS AND HAS A MELLOW, ULTE-LIKE QUALITY.

BIT 5 SAWTOOTH WAVEFORM: WHEN SET THE SAWTOOTH WAVEFORM OUTPUT IS ELECTED. THE SAWTOOTH WAVEFORM IS RICH IN EVEN AND ODD HARMONICS AND HAS A RIGHT, BRASSY QUALITY.

BIT 6 PULSE WAVEFORM: WHEN SET THE PULSE WAVEFORM OUTPUT OF OSC 1 IS ELECTED. THE HARMONIC QUALITY OF THIS WAVEFORM CAN BE ADJUSTED BY THE PULSE IDTH REGISTERS, PRODUCING A TONE FROM A BRIGHT, HOLLOW SQUARE WAVE TO A NASAL, EEDY PULSE. SWEEPING THE PULSE PRODUCES A DYNAMIC "PHASING" EFFECT.

BIT 7 NOISE WAVEFORM: WHEN SET THE NOISE OUTPUT WAVEFORM OF OSC 1 IS ELECTED. THIS OUTPUT IS A RANDOM SIGNAL WHICH CHANGES AT THE FREQUENCY OF OSC . THE SOUN QUALITY CAN BE VARIED FROM A LOW RUMBLING TO A HISSING WHITE NOISE.

EGISTER 5 (S+5) IS THE ATTACK/DECAY REGISTER.

BIT 4-7 ATTACK RATE(VALUE FROM 0 TO 15, SEE TABLE)

BIT 0-3 DECAY RATE (VALUE FROM 0 TO 15, SEE TABLE)

EGISTER 6 (S+6) IS THE SUSTAIN/RELEASE REGISTER.

BIT 4-7 SUSTAIN RATE(AMPLITUDE VALUE DURING SUSTAIN 0=MIN, 15=MAX)

BIT 0-3 RELEASE RATE(VALUE FROM 0 TO 15, SEE TABLE)

ABLE OF RATES:

VALUE	ATTACK RATE	DECAY/RELEASE RATE
0	2mS	6mS
1	8mS	24mS
2	16mS	48mS
3	24mS	72mS
4	38mS	114mS
5	56mS	168mS
6	68mS	204mS
7	80mS	240mS
8	100mS	300mS
9	250mS	750mS
10	500mS	1.5S
11	800mS	2.4S
12	1S	3S
13	3S	9S
14	5S	15S
15	8S	24S

EGISTERS 21 AND BITS 0-2 OF REGISTER 22 CONTROL THE CUTOFF FREQUENCY FOR THE ROGRAMMABLE FILTER.

FCout=(30+FCin*5.8)Hz

EGISTER 23 IS THE RESONANCE/FILTER CONTROL.

BIT 4-7 CONTROL THE RESONANCE OF THE FILTER. THERE ARE 16 SETTINGS FROM 0 NO RESONANCE) TO 15 (MAXIMUM RESONANCE).

BIT 0-3 DETERMINE SIGNALS TO BE ROUTED THROUGH FILTER:

BIT 0 VOICE 1, WHEN SET SIGNAL WILL BE PROCESSED, UNSET SIGNAL WILL PPEAR DIRECTLY AT OUTPUT.

BIT 1 SAME FOR VOICE 2

BIT 2 SAME FOR VOICE 3

BIT 3 SAME FOR EXTERNAL INPUT

EGISTER 24 IS THE FILTER MODE/VOLUME CONTROL.

BIT 4-7 SELECTS VARIOUS FILTER MODES.

BIT 4 WHEN SET LOW PASS FILTER IS SELECTED.(COMPONENTS BELOW CUTOFF ARE NALTERED, COMPONENTS ABOVE CUTOFF ARE ATTENUATED AT 12dB/OCTAVE)

BIT 5 WHEN SET BAND PASS FILTER IS SELECTED.(ALL FREQUENCY COMPONENTS BOVE AND BELOW CUTOFF ARE ATTENUATED AT 6dB/OCTAVE)

BIT 6 WHEN SET HIGH PASS FILTER IS SELECTED.(COMPONENTS ABOVE CUTOFF ARE NALTERED, COMPONENTS BELOW CUTOFF ARE ATTENUATED AT 12dB/OCTAVE)

BIT 7 WHEN SET VOICE 3 IS DISCONNECTED FROM AUDIO PATH.(THIS ALLOWS OICE 3 TO BE USED FOR MODULATION WITHOUT ANY UNDESIREABLE OUTPUT)

BIT 0-3 SELECT 1 OF 16 OVERALL VOLUME LEVELS FOR THE FINAL COMPOSUTE AUDIO UTPUT

EGISTER 25 IS AN A/D CONVERTER FOR POTX (PIN 24).

EGISTER 26 IS AN A/D CONVERTER FOR POTY (PIN 23).

EGISTER 27 IS OSCILLATOR 3/RANDOM NUMBER GENERATOR REGISTER. IT ALLOWS THE ICROPROCESSOR TO READ THE UPPER 8 OUTPUT BITS OF OSCILLATOR 3. THE CHARACTER F THE NUMBER GENERATED IS DIRECTLY RELATED TO THE WAVEFORM SELECTED.

IF THE SAWTOOTH WAVEFORM IS SELECTED THE REGISTER PRESENTS A SERIES OF UMBERS INCREMENTING FORM 0 TO 255 AT A RATE DETERMINED BY OSCILLATOR 3.

IF THE TRIANGLE WAVEFORM IS SELECTED, THE NUMBER WILL INCREMENT FROM 0 TO 55 AND THEN DECREMENT BACK TO ZERO.

IF THE PULSE WAVEFORM IS SELECTED, THE NUMBER WILL JUMP BETWEEN 0 AND 255.

IF THE NOISE WAVEFORM IS GENERATED, A RANDOM NUMBER WILL BE GENERATED.

EGISTER 28 IS THE SAME AS OSCILLATOR 3 BUT IT ALLOWS THE MICROPROCESSOR TO READ HE OUTPUT OF THE VOICE 3 ENVELOPE GENERATOR. THIS OUTPUT CAN BE ADDED TO THE ILTER FREQUENCY TO PRODUCE HARMONIC ENVELOPES, WAH, AND SIMILAR EFFECTS.

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6510 MICROPROCESSOR WITH I/O

PRELIMINARY

DESCRIPTION

The 6510 is a low-cost microcomputer system capable of solving a broad range of small-systems and peripheral-control problems at minimum cost to the user.

An 8-bit Bi-Directional I/O Port is located on-chip with the Output Register at Address 0 0 0 1 and the Data-Direction Register at Address 0 0 0 0. The I/O Port is bit-by-bit programmable.

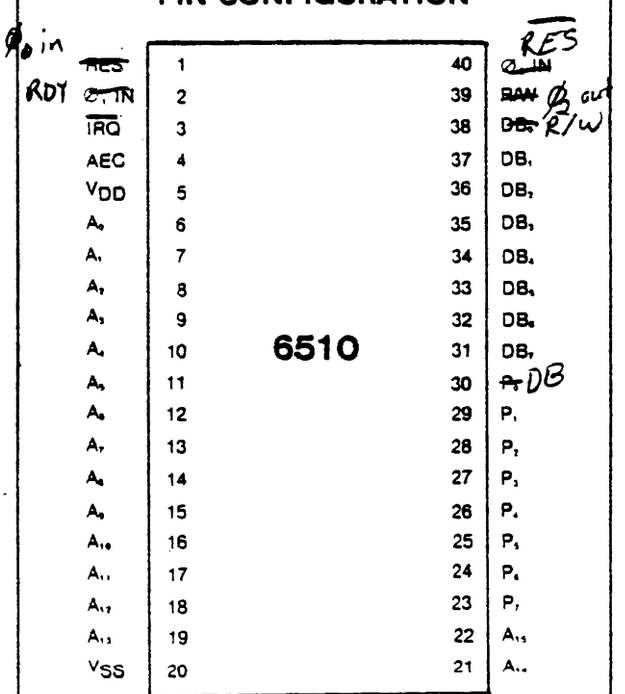
The Three-State sixteen-bit Address Bus allows Direct Memory Accessing (DMA) and multi-processor systems sharing a common memory.

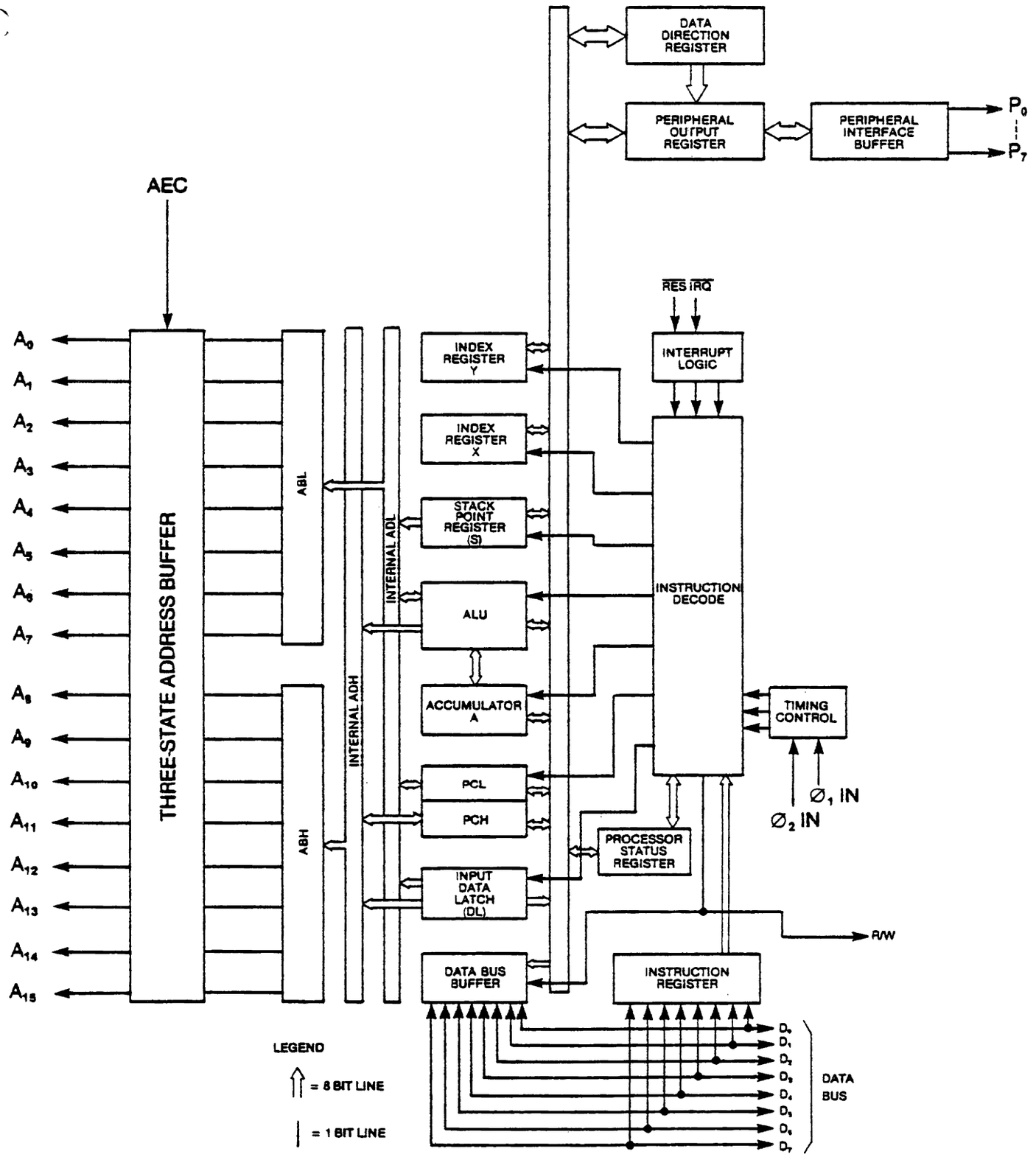
The internal processor architecture is identical to the MOS Technology 6502 to provide software compatibility.

FEATURES OF THE 6510 . . .

- 8-Bit Bi-Directional I/O Port
- Single +5 volt supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- 8 Bit Bi-Directional Data Bus
- Addressable memory range of up to 65K bytes
- Direct memory access capability
- Bus compatible with M6800
- Pipeline architecture
- 1 MHz and 2MHz operation
- Use with any type or speed memory

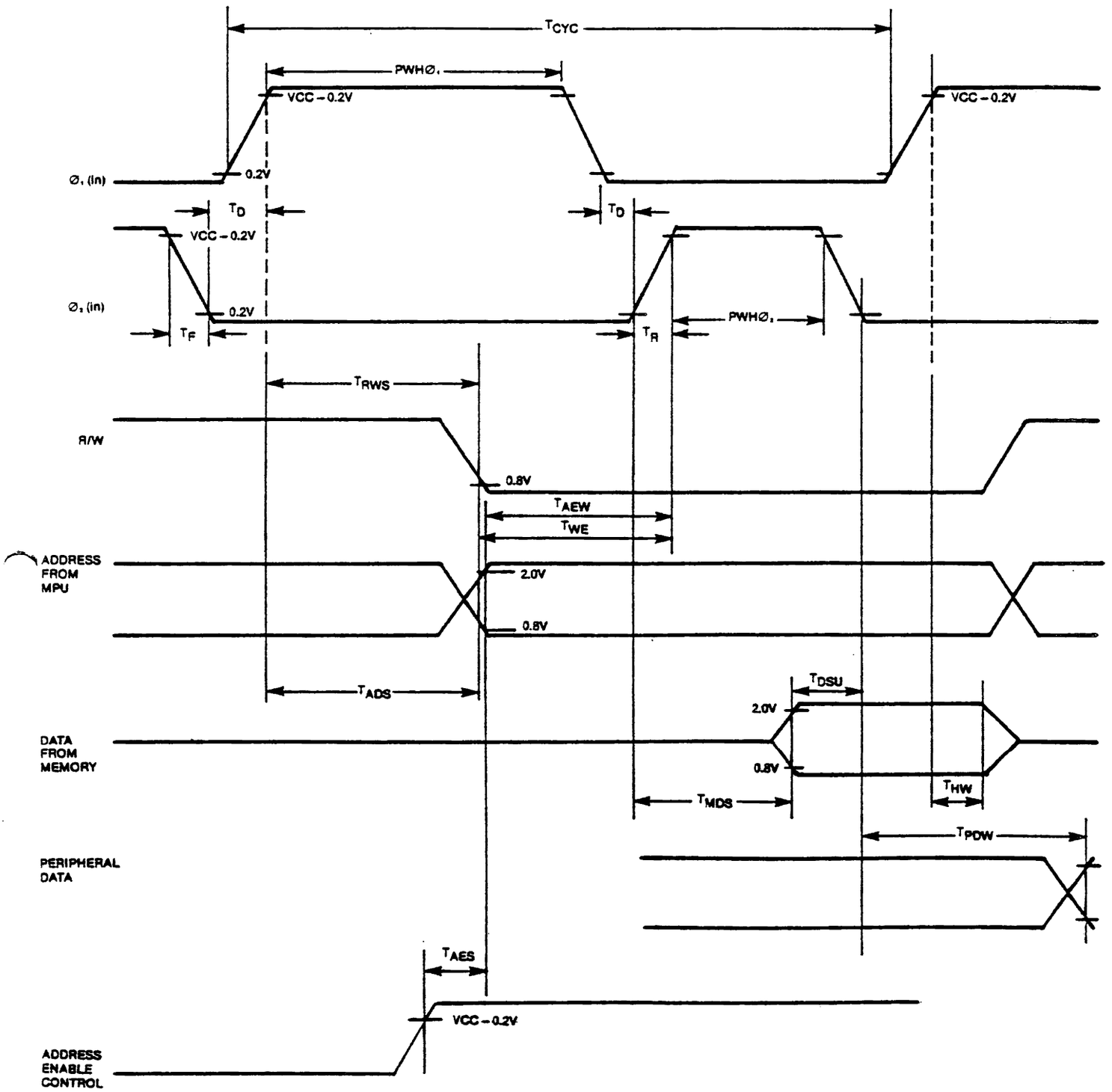
PIN CONFIGURATION





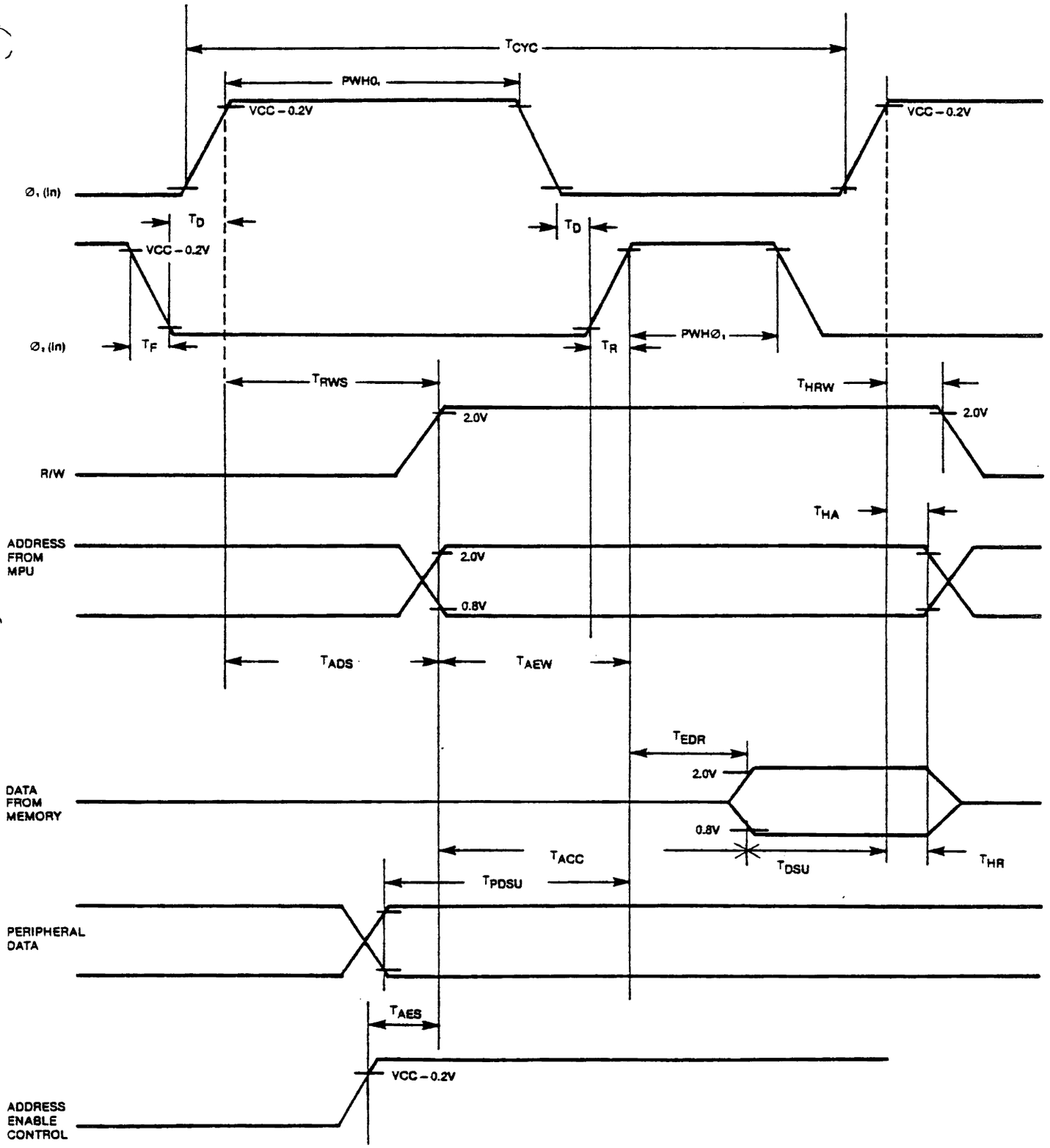
6510 BLOCK DIAGRAM

CLOCK TIMING



TIMING FOR WRITING DATA TO MEMORY OR PERIPHERALS

CLOCK TIMING



TIMING FOR READING DATA FROM MEMORY OR PERIPHERALS

AC CHARACTERISTICS

1 MHz TIMING	2 MHz TIMING

ELECTRICAL CHARACTERISTICS (VCC = 5V ± 5%, VSS = 0V, T_A = 0° – 70°C)

CLOCK TIMING

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Cycle Time	T_{CYC}	1000	—	—	500	—	—	ns
Clock Pulse Width Ø1 (Measured at VCC – 0.2V) Ø2	PWHØ1 PWHØ2	430 470	— —	— —	215 235	— —	— —	ns ns
Fall Time, Rise Time (Measured from 0.2V to VCC – 0.2V)	T_F, T_R	—	—	25	—	—	15	ns
Delay Time between Clocks (Measured at 0.2V)	T_D	0	—	—	0	—	—	ns

READ/WRITE TIMING (LOAD = 1TTL)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Read/Write Setup Time from 6508	T_{RWS}	—	100	300	—	100	150	ns
Address Setup Time from 6508	T_{ADS}	—	100	300	—	100	150	ns
Memory Read Access Time	T_{ACC}	—	—	575	—	—	300	ns
Data Stability Time Period	T_{DSU}	100	—	—	50			ns
Data Hold Time-Read	T_{HR}		—	—				ns
Data Hold Time-Write	T_{HW}	10	30	—	10	30		ns
Data Setup Time from 6510	T_{MDS}	—	150	200	—	75	100	ns
Address Hold Time	T_{HA}	10	30	—	10	30		ns
R/W Hold Time	T_{HRW}	10	30	—	10	30		ns
Delay Time, Address valid to Ø2 positive transition	T_{AEW}	180	—	—				ns
Delay Time, Ø2 positive transition to Data valid on bus	T_{EDR}	—	—	395				ns
Delay Time, Data valid to Ø2 negative transition	T_{DSU}	300	—	—				ns
Delay Time, R/W negative transition to Ø2 positive transition	T_{WE}	130	—	—				ns
Delay Time, Ø2 negative transition to Peripheral Data valid	T_{PDW}	—	—	1				µs
Peripheral Data Setup Time	T_{PDSU}	300	—	—				ns
Address Enable Setup Time	T_{AES}			60			60	ns

ADDRESSING MODES

ACCUMULATOR ADDRESSING—This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING—In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING—In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

ZERO PAGE ADDRESSING—The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING—(X, Y indexing)—This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING—(X, Y indexing)—This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X and Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING—In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING—Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is −128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING—In indexed indirect addressing (referred to as [Indirect, X]), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING—In indirect indexed addressing (referred to as [Indirect, Y]). the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT—The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

INSTRUCTION SET—ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift left One Bit (Memory or Accumulator)
BCC	Branch on Carry Clear
BCS	Branch on Carry Set
BEQ	Branch on Result Zero
BIT	Test Bits in Memory with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
BRK	Force Break
BVC	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive-or" Memory with Accumulator
INC	Increment Memory by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
NOP	No Operation
ORA	"OR" Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Register
TYA	Transfer Index Y to Accumulator

SIGNAL DESCRIPTION

Clocks ($\varnothing_1$, $\varnothing_2$)
The 6510 requires a two phase non-overlapping clock that runs at the Vcc voltage level.

Address Bus (A_0-A_{15})
These outputs are TTL compatible, capable of driving one standard TTL load and 130 pf.

Data Bus (D_0-D_7)
Eight pins are used for the data bus. This is a Bi-Directional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pf.

Reset
This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After Vcc reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

Interrupt Request ($\overline{IRQ}$)
This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses.

Address Enable Control (AEC)
The Address Bus is valid only when the Address Enable Control line is high. When low, the Address Bus is in a high-impedance state. This feature allows easy DMA and multiprocessor systems.

I/O Port (P_0-P_7)
Eight pins are used for the peripheral port, which can transfer data to or from peripheral devices. The Output Register is located in RAM at Address 0001, and the Data Direction Register is at Address 0000. The outputs are capable at driving one standard TTL load and 130 pf.

Read/Write (R/W)
This signal is generated by the microprocessor to control the direction of data transfers on the Data Bus. This line is high except when the microprocessor is writing to memory or a peripheral device.

6510 CHARACTERISTICS

MAXIMUM RATINGS

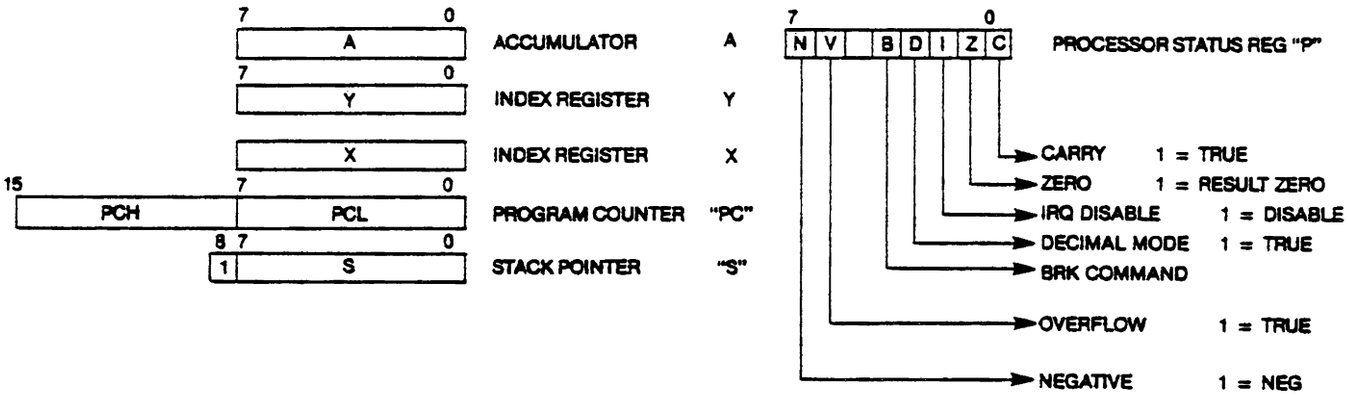
RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	Vcc	−0.3 to +7.0	Vdc
INPUT VOLTAGE	Vin	−0.3 to +7.0	Vdc
OPERATING TEMPERATURE	T_A	0 to +70	°C
STORAGE TEMPERATURE	T_{STG}	−55 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, Vss = 0, T_A = 0° to + 70°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage					
ϕ_1, ϕ_2(in)	VIH	Vcc - 0.2	—	Vcc + 1.0V	Vdc
Input High Voltage					
$\overline{RES}$, P_0-P,$\overline{IRQ}$, Data		Vss + 2.0	—	—	Vdc
Input Low Voltage					
ϕ_1, ϕ_2(In)	VIL	Vss - 0.3	—	Vss + 0.2	Vdc
$\overline{RES}$, P_0-P, $\overline{IRQ}$, Data		—	—	Vss + 0.8	Vdc
Input Leakage Current (V_{In} = 0 to 5.25V, Vcc = 5.25V)					
Logic	Iin	—	—	2.5	μA
ϕ_1, ϕ_2(in)		—	—	100	μA
Three State (Off State) Input Current (V_{In} = 0.4 to 2.4V, Vcc = 5.25V)					
Data Lines	ITSI	—	—	10	μA
Output High Voltage (I_{OH} = -100μAdc, Vcc = 4.75V)					
Data, A0-A15, R/W, P_0-P,	VOH	Vss + 2.4	—	—	Vdc
Out Low Voltage (I_{OL} = 1.6mAdc, Vcc = 4.75V)					
Data, A0-A15, R/W, P_0-P,	VOL	—	—	Vss + 0.4	Vdc
Power Supply Current	ICC	—	125		mA
Capacitance	C				pF
V_{In} = O, T_A = 25°C, f = 1MHz)					
Logic, P_0-P,	C_{in}	—	—	10	
Data		—	—	15	
A0-A15, R/W	C_{out}	—	—	12	
ϕ_1	C_{ϕ_1}	—	30	50	
ϕ_2	C_{ϕ_2}	—	50	80	

PROGRAMMING MODEL



INSTRUCTION SET — OP CODES, Execution Time, Memory Requirements

MNEMONIC	OPERATION	IMMEDIATE OP	IMMEDIATE N	IMMEDIATE #	ABSOLUTE OP	ABSOLUTE N	ABSOLUTE #	ZERO PAGE OP	ZERO PAGE N	ZERO PAGE #	ACCUM OP	ACCUM N	ACCUM #	IMPLIED OP	IMPLIED N	IMPLIED #	(IND,X) OP	(IND,X) N	(IND,X) #	(IND),Y OP	(IND),Y N	(IND),Y #	ZERO PAGE,X OP	ZERO PAGE,X N	ZERO PAGE,X #	ABS,X OP	ABS,X N	ABS,X #	ABS,Y OP	ABS,Y N	ABS,Y #	RELATIVE OP	RELATIVE N	RELATIVE #	INDIRECT OP	INDIRECT N	INDIRECT #	ZERO PAGE,Y OP	ZERO PAGE,Y N	ZERO PAGE,Y #	CONDITION CODES N	Z	C	I	D	V
A D C	A+M+C→A (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										✓	✓	✓	-	-	✓
A N D	A∧M→A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										✓	✓	-	-	-	-
A S L	C ← 7 6 5 4 3 2 1 0 ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													✓	✓	✓	-	-	-
B C C	BRANCH ON C=0 (2)																														90	2	2							-	-	-	-	-	-
B C S	BRANCH ON C=1 (2)																														B0	2	2							-	-	-	-	-	-
B E Q	BRANCH ON Z=1 (2)																														F0	2	2							-	-	-	-	-	-
B I T	A∧M (3)				2C	4	3	24	3	2																														M7	M6	-	-	-	M6
B M I	BRANCH ON N=1 (2)																														30	2	2							-	-	-	-	-	-
B N E	BRANCH ON Z=0 (2)																														D0	2	2							-	-	-	-	-	-
B P L	BRANCH ON N=0 (2)																														10	2	2							-	-	-	-	-	-
B R K	(See Fig. 11)													00	7	1																								-	-	-	1	-	-
B V C	BRANCH ON V=0 (2)																														50	2	2							-	-	-	-	-	-
B V S	BRANCH ON V=1 (2)																														70	2	2							-	-	-	-	-	-
C L C	0→C													18	2	1																								-	-	0	-	-	-
C L D	0→D													D8	2	1																								-	-	-	-	0	-
C L I	0→I													58	2	1																								-	-	-	0	-	-
C L V	0→V													B8	2	1																								-	-	-	-	-	0
C M P	A−M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										✓	✓	✓	-	-	-
C P X	X−M	E0	2	2	EC	4	3	E4	3	2																														✓	✓	✓	-	-	-
C P Y	Y−M	C0	2	2	CC	4	3	C4	3	2																														✓	✓	✓	-	-	-
D E C	M−1→M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													✓	✓	-	-	-	-
D E X	X−1→X													CA	2	1																								✓	✓	-	-	-	-
D E Y	Y−1→Y													88	2	1																								✓	✓	-	-	-	-
E O R	A⊻M→A	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										✓	✓	-	-	-	-
I N C	M+1→M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													✓	✓	-	-	-	-
I N X	X+1→X													E8	2	1																								✓	✓	-	-	-	-
I N Y	Y+1→Y													C8	2	1																								✓	✓	-	-	-	-
J M P	JUMP TO NEW LOC.				4C	3	3																											6C	5	3							-	-	-	-	-	-
J S R	PUSH (PC+2), (PC+1)→PCL, (PC+2)→PCH				20	6	3																																							
L D A	M→A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										✓	✓	-	-	-	-
L D X	M→X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2	✓	✓	-	-	-	-
L D Y	M→Y	A0	2	2	AC	4	3	A4	3	2																														✓	✓	-	-	-	-
L S R	0→ 7 6 5 4 3 2 1 0 →C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0	✓	✓	-	-	-
O R A	A∨M→A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										✓	✓	-	-	-	-
P H A	A→M$_S$ S−1→S													48	3	1																								-	-	-	-	-	-
P L A	S+1→S M$_S$→A													68	4	1																								✓	✓	-	-	-	-
R O L	7 6 5 4 3 2 1 0 ←C				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													✓	✓	✓	-	-	-
R O R	C→ 7 6 5 4 3 2 1 0				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													✓	✓	✓	-	-	-
R T I	(See Fig.2) RTRN INTR													40	6	1																								✓	✓	✓	-	-	-
R T S	(See Fig.2) RTRN SUB													60	6	1																								-	-	-	-	-	-
S E C	1→C													38	2	1																								-	-	1	-	-	-
S E D	1→D													F8	2	1																								-	-	-	-	1	-
S E I	1→I													78	2	1																								-	-	-	1	-	-
S T A	A→M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										-	-	-	-	-	-
S T X	X→M				8E	4	3	86	3	2																														96	4	2	-	-	-	-	-	-
S T Y	Y→M				8C	4	3	84	3	2													94	4	2																-	-	-	-	-	-
T A X	A→X													AA	2	1																								✓	✓	-	-	-	-
T S X	S→X													BA	2	1																								✓	✓	-	-	-	-
T X A	X→A													8A	2	1																								✓	✓	-	-	-	-
T X S	X→S													9A	2	1																								-	-	-	-	-	-
T Y A	Y→A													98	2	1																								✓	✓	-	-	-	-

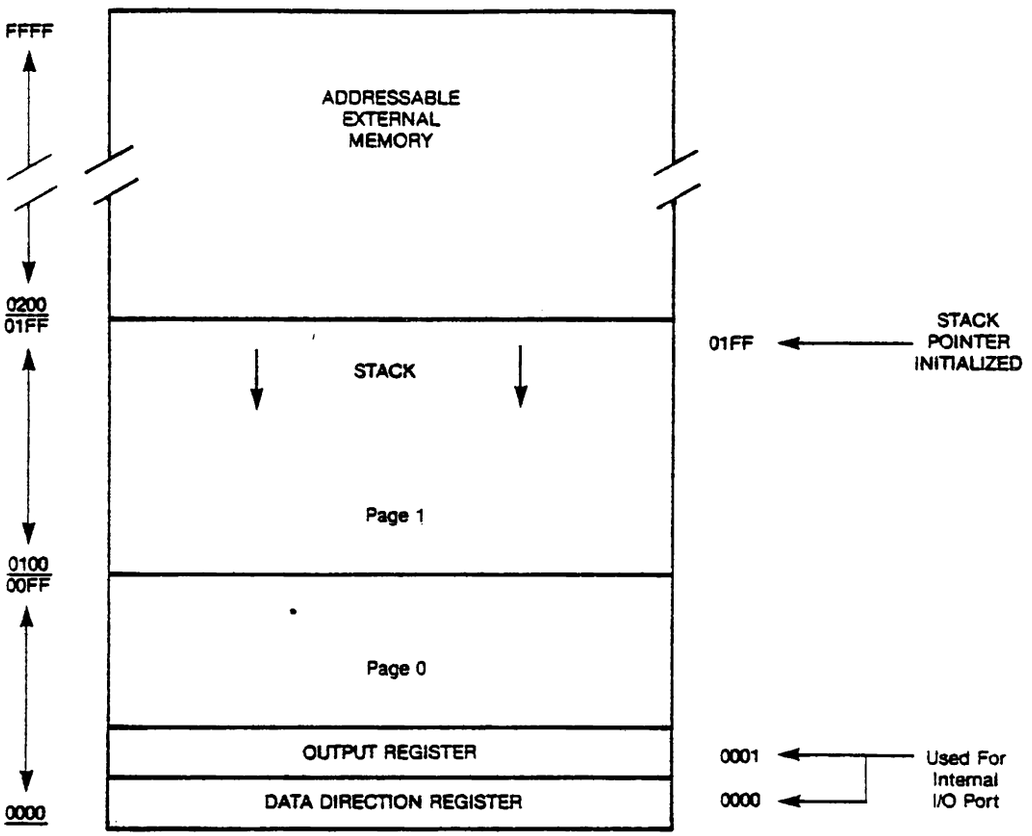
(1) ADD 1 TO "N" IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO "N" IF BRANCH OCCURS TO SAME PAGE. ADD 2 TO "N" IF BRANCH OCCURS TO DIFFERENT PAGE.
(3) CARRY NOT=BORROW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID. ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT.

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
M$_S$ MEMORY PER STACK POINTER

+ ADD
− SUBTRACT
∧ AND
∨ OR
⊻ EXCLUSIVE OR
/ MODIFIED
- NOT MODIFIED
M$_7$ MEMORY BIT 7
M$_6$ MEMORY BIT 6

N NO CYCLES
NO. BYTES

Note: Commodore Semiconductor Group cannot assume liability for the use of undefined OP Codes



6510 MEMORY MAP

APPLICATIONS NOTES

Locating the Output Register at the internal I/O Port in Page Zero enhances the powerful Zero Page Addressing instructions of the 6510.

By assigning the I/O Pins as inputs (using the Data Direction Register) the user has the ability to change the contents of address 0001 (the Output Register) using peripheral devices. The ability to change these contents using peripheral inputs, together with Zero Page Indirect Addressing instructions, allows novel and versatile programming techniques not possible earlier.

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USER'S NOTES

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6526 COMPLEX INTERFACE ADAPTER (CIA)

DESCRIPTION

The 6526 Complex Interface Adapter (CIA) is a 65XX bus compatible peripheral Interface device with extremely flexible timing and I/O capabilities.

FEATURES

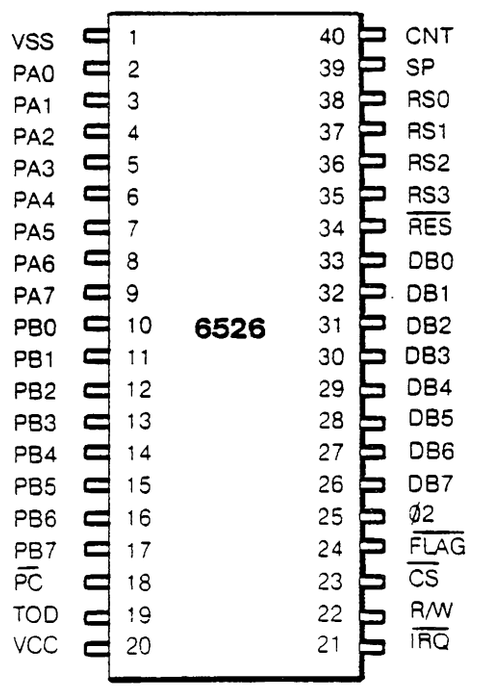
- 16 Individually programmable I/O lines
- 8 or 16-Bit handshaking on read or write
- 2 independent, linkable 16-Bit interval timers
- 24-hour (AM/PM) time of day clock with programmable alarm
- 8-Bit shift register for serial I/O
- 2TTL Load capability
- CMOS compatible I/O lines
- 1 or 2 MHz operation available

ORDERING INFORMATION

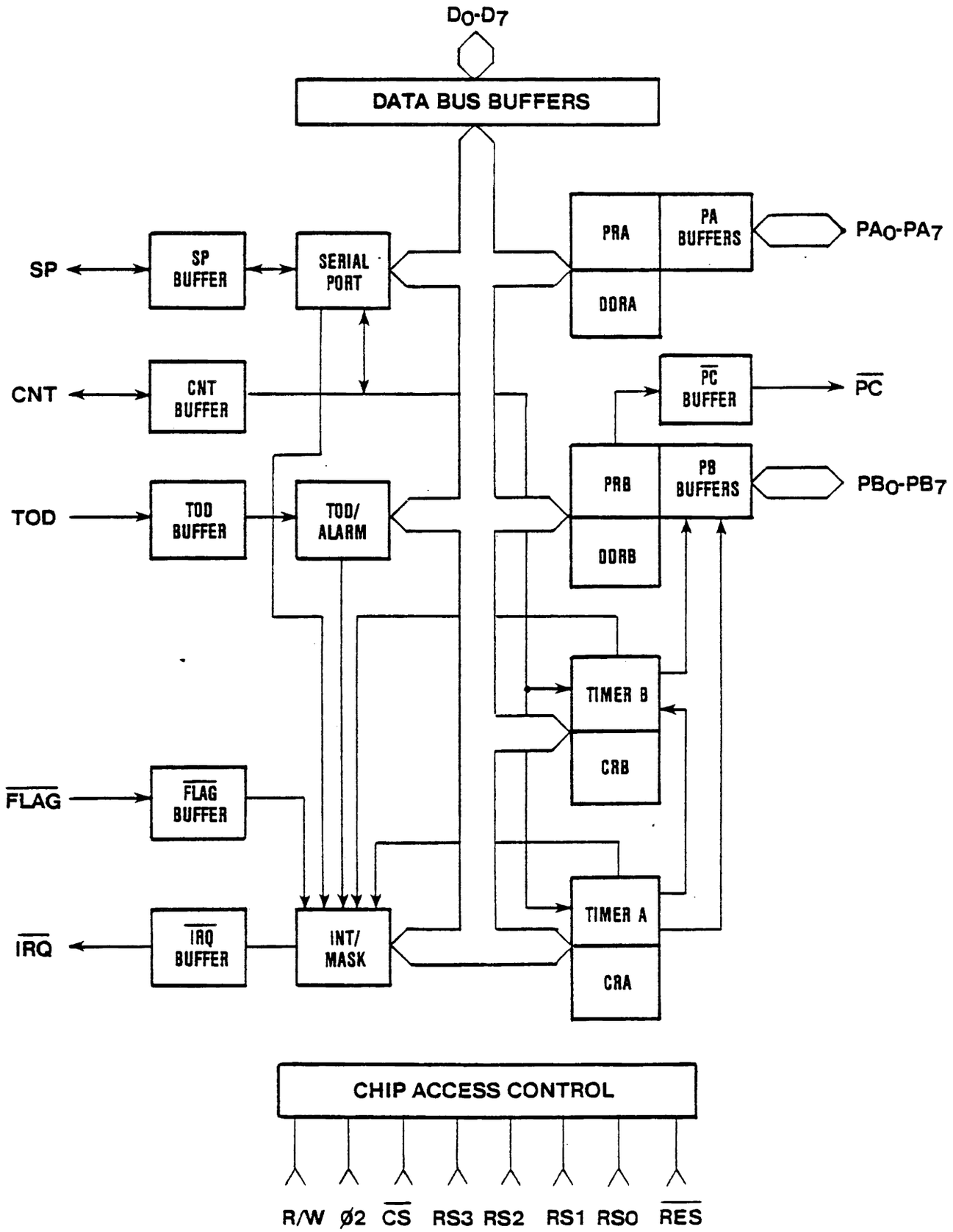
MXS 6526

- FREQUENCY RANGE
  - NO SUFFIX = 1MHz
  - A = 2MHz
- PACKAGE DESIGNATOR
  - C = CERAMIC
  - P = PLASTIC

PIN CONFIGURATION



6526
BLOCK DIAGRAM



MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input/Output Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	−55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

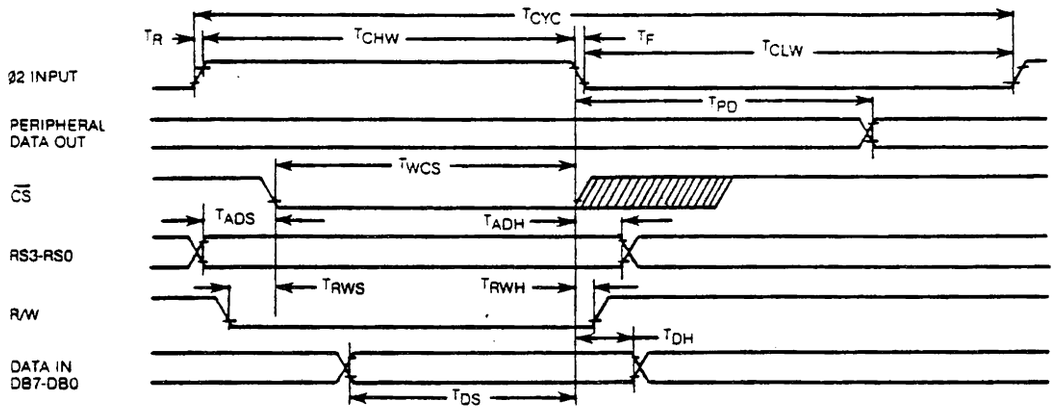
COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

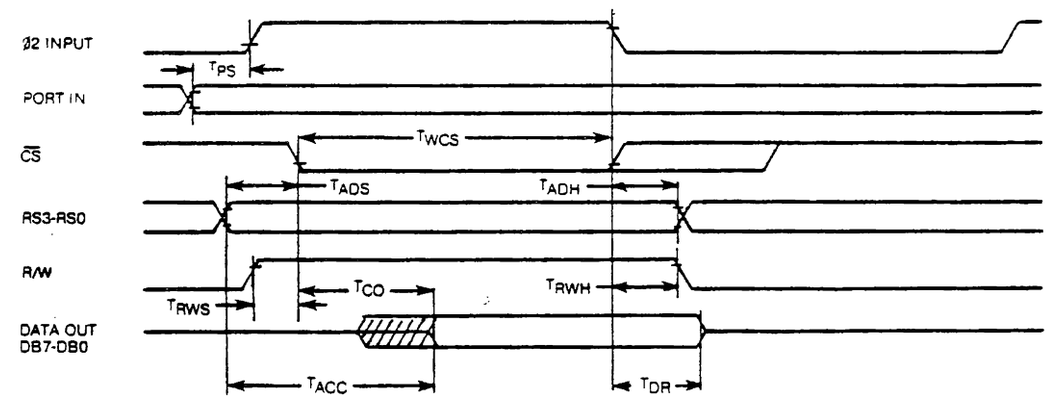
ELECTRICAL CHARACTERISTICS (V_{CC} ± 5%, VSS = 0v, T_A = 0-70°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	+ 2.4	—	V_{CC}	V
Input Low Voltage	V_{IL}	− 0.3	—	—	V
Input Leakage Current; V_{IN} = V_{SS} + 5v (TOD, R/W, $\overline{FLAG}$, Ø2, $\overline{RES}$, RS0-RS3, $\overline{CS}$)	I_{IN}	—	1.0	2.5	µA
Port Input Pull-up Resistance	R_{PI}	3.1	5.0	—	KΩ
Output Leakage Current for High Impedance State (Three State); V_{IN} = 4v to 2.4v; (DB0-DB7, SP, CNT, $\overline{IRQ}$)	I_{TSI}	—	± 1.0	± 10.0	µA
Output High Voltage VCC=MIN, I_{LOAD} < −200uA (PA0-PA7, $\overline{PC}$ PB0-PB7, DB0-DB7)	V_{OH}	+ 2.4	—	V_{CC}	V
Output Low Voltage VCC = MIN, I_{LOAD} < 3.2mA	V_{OL}	—	—	+ 0.40	V
Output High Current (Sourcing); VOH > 2.4v (PA0-PA7, PB0-PB7, PC, DB0-DB7)	I_{OH}	−200	−1000	—	µA
Output Low Current (Sinking); VOL < .4 v (PA0-PA7, $\overline{PC}$, PB0-PB7, DB0-DB7)	I_{OL}	3.2	—	—	mA
Input Capacitance	C_{IN}	—	7	10	pf
Output Capacitance	C_{OUT}	—	7	10	pf
Power Supply Current	I_{CC}	—	70	100	mA

6526 WRITE TIMING DIAGRAM



6526 READ TIMING DIAGRAM



6526 INTERFACE SIGNALS

Ø2 — Clock Input

The Ø2 clock is a TTL compatible input used for internal device operation and as a timing reference for communicating with the system data bus.

$\overline{CS}$ — Chip Select Input

The $\overline{CS}$ input controls the activity of the 6526. A low level on $\overline{CS}$ while Ø2 is high causes the device to respond to signals on the R/W and address (RS) lines. A high on $\overline{CS}$ prevents these lines from controlling the 6526. The $\overline{CS}$ line is normally activated (low) at Ø2 by the appropriate address combination.

R/W — Read/Write Input

The R/W signal is normally supplied by the microprocessor and controls the direction of data transfers of the 6526. A high on R/W indicates a read (data transfer out of the 6526), while a low indicates a write (data transfer into the 6526).

RS3-RS0 — Address Inputs

The address inputs select the internal registers as described by the Register Map.

DB7-BD0 — Data Bus Inputs/Outputs

The eight data bus pins transfer information between the 6526 and the system data bus. These pins are high impedance inputs unless $\overline{CS}$ is low and R/W and Ø2 are high, to read the device. During this read, the data bus output buffers are enabled, driving the data from the selected register onto the system data bus.

$\overline{IRQ}$ — Interrupt Request Output

$\overline{IRQ}$ is an open drain output normally connected to the processor interrupt input. An external pullup resistor holds the signal high, allowing multiple $\overline{IRQ}$ outputs to be connected together. The $\overline{IRQ}$ output is normally off (high impedance) and is activated low as indicated in the functional description.

$\overline{RES}$ — Reset Input

A low on the $\overline{RES}$ pin resets all internal registers. The port pins are set as inputs and port registers to zero (although a read of the ports will return all highs because of passive pullups). The timer control registers are set to zero and the timer latches to all ones. All other registers are reset to zero.

CONTROL REGISTERS

There are two control registers in the 6526, CRA and CRB. CRA is associated with TIMER A and CRB is associated with TIMER B. The register format is as follows:

CRA:

Bit	Name	Function
0	START	1=START TIMER A, 0=STOP TIMER A. This bit is automatically reset when underflow occurs during one-shot mode.
1	PBON	1=TIMER A output appears on PB6, 0=PB6 normal operation.
2	OUTMODE	1=TOGGLE, 0=PULSE
3	RUNMODE	1=ONE-SHOT, 0=CONTINUOUS
4	LOAD	1=FORCE LOAD (this is a STROBE input, there is no data storage, bit 4 will always read back a zero and writing a zero has no effect).
5	INMODE	1=TIMER A counts positive CNT transitions, 0=TIMER A counts Ø2 pulses.
6	SPMODE	1=SERIAL PORT output (CNT sources shift clock), 0=SERIAL PORT input (external shift clock required).
7	TODIN	1=50 Hz clock required on TOD pin for accurate time, 0=60 Hz clock required on TOD pin for accurate time.

CRB:

Bit	Name	Function
		(Bits CRB0-CRB4 are identical to CRA0-CRA4 for TIMER B with the exception that bit 1 controls the output of TIMER B on PB7).
5,6	INMODE	Bits CRB5 and CRB6 select one of four input modes for TIMER B as:

CRB6	CRB5	
0	0	TIMER B counts Ø2 pulses.
0	1	TIMER B counts positive CNT transistions.
1	0	TIMER B counts TIMER A underflow pulses.
1	1	TIMER B counts TIMER A underflow pulses while CNT is high.

7 ALARM — 1=writing to TOD registers sets ALARM, 0=writing to TOD registers sets TOD clock.

REG	NAME	TOD IN	SP MODE	IN MODE	LOAD	RUN MODE	OUT MODE	PB ON	START
E	CRA	0=60Hz	0=INPUT	0=Ø2	1=FORCE LOAD	0=CONT.	0=PULSE	0=PB6 OFF	0=STOP
		1=50Hz	1=OUTPUT	1=CNT	(STROBE)	1=O.S.	1=TOGGLE	1=PB6 ON	1=START

TA

REG	NAME	ALARM	IN MODE		LOAD	RUN MODE	OUT MODE	PB ON	START
F	CRB	0=TOD	0	0=Ø2	1=FORCE LOAD	0=CONT.	0=PULSE	0=PB7 OFF	0=STOP
			0	1=CNT					
			1	0=TA					
		1= ALARM	1	1=CNT•TA	(STROBE)	1=O.S.	1=TOGGLE	1=PB7 ON	1=START

TB

All unused register bits are unaffected by a write and are forced to zero on a read.

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6526 TIMING CHARACTERISTICS

Symbol	Characteristic	1MHz MIN	1MHz MAX	2MHz MIN	2MHz MAX	Unit
	ϕ_2 Clock					
T_{CYC}	Cycle Time	1,000	20,000	500	20,000	nS
T_R, T_F	Rise and Fall Time	—	25	—	25	nS
T_{CHW}	Clock Pulse Width (High)	420	10,000	200	10,000	nS
T_{CLW}	Clock Pulse Width (Low)	420	10,000	200	10,000	nS
	Write Cycle					
T_{PD}	Output Delay From ϕ_2	—	1,000	—	500	nS
T_{WCS}	$\overline{CS}$ low while ϕ_2 high	420	—	200	—	nS
T_{ADS}	Address Setup Time	0	—	0	—	nS
T_{ADH}	Address Hold Time	10	—	5	—	nS
T_{RWS}	R/W Setup Time	0	—	0	—	nS
T_{RWH}	R/W Hold Time	0	—	0	—	nS
T_{DS}	Data Bus Setup Time	150	—	75	—	nS
T_{DH}	Data Bus Hold Time	0	—	0	—	nS
	Read Cycle					
T_{PS}	Port Setup Time	300	—	150	—	nS
T_{WCS}(2)	$\overline{CS}$ low while ϕ_2 high	420	—	20	—	nS
T_{ADS}	Address Setup Time	0	—	0	—	nS
T_{ADH}	Address Hold Time	10	—	5	—	nS
T_{RWS}	R/W Setup Time	0	—	0	—	nS
T_{RWH}	R/W Hold Time	0	—	0	—	nS
T_{ACC}	Data Access from RS3-RS0	—	550	—	275	nS
T_{CO}(3)	Data Access from $\overline{CS}$	—	320	—	150	nS
T_{DR}	Data Release Time	50	—	25	—	nS

NOTES: 1 — All timings are referenced from V_{IL} max and V_{IH} min on inputs and V_{OL} max and V_{OH} min on outputs.
2 — T_{WCS} is measured from the later of Ø2 high or $\overline{CS}$ low. $\overline{CS}$ must be low at least until the end of Ø2 high.
3 — T_{CO} is measured from the later of Ø2 high or $\overline{CS}$ low.
Valid data is available only after the later of T_{ACC} or T_{CO}.

REGISTER MAP

RS3	RS2	RS1	RS0	REG		
0	0	0	0	0	PRA	PERIPHERAL DATA REG A
0	0	0	1	1	PRB	PERIPHERAL DATA REG B
0	0	1	0	2	DDRA	DATA DIRECTION REG A
0	0	1	1	3	DDRB	DATA DIRECTION REG B
0	1	0	0	4	TA LO	TIMER A LOW REGISTER
0	1	0	1	5	TA HI	TIMER A HIGH REGISTER
0	1	1	0	6	TB LO	TIMER B LOW REGISTER
0	1	1	1	7	TB HI	TIMER B HIGH REGISTER
1	0	0	0	8	TOD 10THS	10THS OF SECONDS REGISTER
1	0	0	1	9	TOD SEC	SECONDS REGISTER
1	0	1	0	A	TOD MIN	MINUTES REGISTER
1	0	1	1	B	TOD HR	HOURS — AM/PM REGISTER
1	1	0	0	C	SDR	SERIAL DATA REGISTER
1	1	0	1	D	ICR	INTERRUPT CONTROL REGISTER
1	1	1	0	E	CRA	CONTROL REG A
1	1	1	1	F	CRB	CONTROL REG B

6526 FUNCTIONAL DESCRIPTION

I/O Ports (PRA, PRB, DDRA, DDRB).

Ports A and B each consist of an 8-bit Peripheral Data Register (PR) and an 8-bit Data Direction Register (DDR). If a bit in the DDR is set to the corresponding bit in the PR is an output, if a DDR bit is set to a zero, the corresponding PR bit is defined as an input. On a READ, the PR reflects the information present on the actual port pins (PA0-PA7, PB0-PB7) for both input and output bits. Port A and Port B have passive pull-up devices as well as active pull-ups, providing both CMOS and TTL compatibility. Both ports have two TTL load drive capability. In addition to normal I/O operation, PB6 and PB7 also provide timer output functions.

Handshaking

Handshaking on data transfers can be accomplished using the $\overline{PC}$ output pin and the $\overline{FLAG}$ input pin. $\overline{PC}$ will go low for one cycle following a read or write of PORT B. This signal can be used to indicate "data ready" at PORT B or "data accepted" from PORT B. Handshaking on 16-bit data transfers (using both PORT A and PORT B) is possible by always reading or writing PORT A first. $\overline{FLAG}$ is a negative edge sensitive input which can be used for receiving the $\overline{PC}$ output from another 6526, or as a general purpose interrupt input. Any negative transition on $\overline{FLAG}$ will set the $\overline{FLAG}$ interrupt bit.

REG	NAME	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	PRA	PA_7	PA_6	PA_5	PA_4	PA_3	PA_2	PA_1	PA_0
1	PRB	PB_7	PB_6	PB_5	PB_4	PB_3	PB_2	PB_1	PB_0
2	DDRA	DPA_7	DPA_6	DPA_5	DPA_4	DPA_3	DPA_2	DPA_1	DPA_0
3	DDRB	DPB_7	DPB_6	DPB_5	DPB_4	DPB_3	DPB_2	DPB_1	DPB_0

Interval Timers (Timer A, Timer B)

Each interval timer consists of a 16-bit read-only Timer Counter and a 16-bit write-only Timer Latch. Data written to the timer are latched in the Timer Latch, while data read from the timer are the present contents of the Timer Counter. The timers can be used independently or linked for extended operations. The various timer modes allow generation of long time delays, variable width pulses, pulse trains and variable frequency waveforms. Utilizing the CNT input, the timers can count external pulses or measure frequency, pulse width and delay times of external signals. Each timer has an associated control register, providing independent control of the following functions:

Start/Stop

A control bit allows the timer to be started or stopped by the microprocessor at any time.

PB On/Off:

A control bit allows the timer output to appear on a PORT B output line (PB6 for TIMER A and PB7 for TIMER B). This function overrides the DDRB control bit and forces the appropriate PB line to an output.

Toggle/Pulse

A control bit selects the output applied to PORT B. On every timer underflow the output can either toggle or generate a single positive pulse of one cycle duration. The Toggle output is set high whenever the timer is started and is set low by $\overline{RES}$.

One-Short/Continuous

A control bit selects either timer mode. In one-shot mode, the timer will count down from the latched value to zero, generate an interrupt, reload the latched value, then stop. In continuous mode, the timer will count from the latched value to zero, generate an interrupt, reload the latched value and repeat the procedure continuously.

Force Load

A strobe bit allows the timer latch to be loaded into the timer counter at any time, whether the timer is running or not.

Input Mode:

Control bits allow selection of the clock used to decrement the timer. TIMER A can count Ø2 clock pulses or external pulses applied to the CNT pin. TIMER B can count Ø2 pulses, external CNT pulses, TIMER A underflow pulses or TIMER A underflow pulses while the CNT pin is held high.

The timer latch is loaded into the timer on any timer underflow, on a force load or following a write to the high byte of the prescaler while the timer is stopped. If the timer is running, a write to the high byte will load the timer latch, but not reload the counter.

READ (TIMER)

REG	NAME								
4	TA LO	TAL_7	TAL_6	TAL_5	TAL_4	TAL_3	TAL_2	TAL_1	TAL_0
5	TA HI	TAH_7	TAH_6	TAH_5	TAH_4	TAH_3	TAH_2	TAH_1	TAH_0
6	TB LO	TBL_7	TBL_6	TBL_5	TBL_4	TBL_3	TBL_2	TBL_1	TBL_0
7	TB HI	TBH_7	TBH_6	TBH_5	TBH_4	TBH_3	TBH_2	TBH_1	TBH_0

WRITE (PRESCALER)

REG	NAME								
4	TA LO	PAL_7	PAL_6	PAL_5	PAL_4	PAL_3	PAL_2	PAL_1	PAL_0
5	TA HI	PAH_7	PAH_6	PAH_5	PAH_4	PAH_3	PAH_2	PAH_1	PAH_0
6	TB LO	PBL_7	PBL_6	PBL_5	PBL_4	PBL_3	PBL_2	PBL_1	PBL_0
7	TB HI	PBH_7	PBH_6	PBH_5	PBH_4	PBH_3	PBH_2	PBH_1	PBH_0

Time of Day Clock (TOD)

The TOD clock is a special purpose timer for real-time applications. TOD consists of a 24-hour (AM/PM) clock with 1/10th second resolution. It is organized into 4 registers: 10ths of seconds, Seconds, Minutes and Hours. The AM/PM flag is in the MSB of the Hours register for easy bit testing. Each register reads out in BCD format to simplify conversion for driving displays, etc. The clock requires an external 60 Hz or 50 Hz (programmable) TTL level input on the TOD pin for accurate time-keeping. In addition to time-keeping, a programmable ALARM is provided for generating an interrupt at a desired time. The ALARM registers are located at the same addresses as the corresponding TOD registers. Access to the ALARM is governed by a Control Register bit. The ALARM is write-only; any read of a TOD address will read time regardless of the state of the ALARM access bit.

A specific sequence of events must be followed for proper setting and reading of TOD. TOD is automatically stopped whenever a write to the Hours register occurs. The clock will not start again until after a write to the 10ths of seconds register. This assures TOD will always start at the desired time. Since a carry

from one stage to the next can occur at any time with respect to a read operation, a latching function is included to keep all Time Of Day information constant during a read sequence. All four TOD registers latch on a read of Hours and remain latched until after a read of 10ths of seconds. The TOD clock continues to count when the output registers are latched. If only one register is to be read, there is no carry problem and the register can be read "on the fly," provided that any read of Hours is followed by a read of 10ths of seconds to disable the latching.

READ

REG	NAME							
8	TOD 10THS	0	0	0	0	T_8	T_4	T_2	T_1
9	TOD SEC	0	SH_4	SH_2	SH_1	SL_8	SL_4	SL_2	SL_1
A	TOD MIN	0	MH_4	MH_2	MH_1	ML_8	ML_4	ML_2	ML_1
B	TOD HR	PM	0	0	HH	HL_8	HL_4	HL_2	HL_1

WRITE

CRB_7=0 TOD
CRB_7=1 ALARM
(SAME FORMAT AS READ)

Serial Port (SDR)

The serial port is a buffered, 8-bit synchronous shift register system. A control bit selects input or output mode. In input mode, data on the SP pin is shifted into the shift register on the rising edge of the signal applied to the CNT pin. After 8 CNT pulses, the data in the shift register is dumped into the Serial Data Register and an interrupt is generated. In the output mode, TIMER A is used for the baud rate generator. Data is shifted out on the SP pin at ½ the underflow rate of TIMER A. The maximum baud rate possible is Ø2 divided by 4, but the maximum useable baud rate will be determined by line loading and the speed at which the receiver responds to input data. Transmission will start following a write to the Serial Data Register (provided TIMER A is running and in continuous mode). The clock signal derived from TIMER A appears as an output on the CNT pin. The data in the Serial Data Register will be loaded into the shift register then shift out to the SP pin when a CNT pulse occurs. Data shifted out becomes valid on the falling edge of CNT and remains valid until the next falling edge. After 8 CNT pulses, an interrupt is generated to indicate more data can be sent. If the Serial Data Register was loaded with new information prior to this interrupt, the new data will automatically be loaded into the shift register and transmission will continue. If the microprocessor stays one byte ahead of the shift register, transmission will be continuous. If no further data is to be transmitted, after the 8th CNT pulse, CNT will return high and SP will remain at the level of the last data bit transmitted. SDR data is shifted out MSB first and serial input data should also appear in this format.

The bidirectional capability of the Serial Port and CNT clock allows many 6526 devices to be connected to a common serial communication bus on which one 6526 acts as a master, sourcing data and shift clock, while all other 6526 chips act as slaves. Both CNT and SP outputs are open drain to allow such a common bus. Protocol for master/slave selection can be transmitted over the serial bus, or via dedicated handshaking lines.

REG	NAME								
C	SDR	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

Interrupt Control (ICR)

There are five sources of interrupts on the 6526: underflow from TIMER A, underflow from TIMER B, TOD ALARM, Serial Port full/empty and $\overline{FLAG}$. A single register provides masking and interrupt information. The Interrupt Control Register consists of a write-only MASK register and a read-only DATA register. Any interrupt will set the corresponding bit in the DATA register. Any interrupt which is enabled by the MASK register will set the IR bit (MSB) of the DATA register and bring the $\overline{IRQ}$ pin low. In a multi-chip system, the IR bit can be polled to detect which chip has generated an interrupt request. The interrupt DATA register is cleared and the $\overline{IRQ}$ line returns high following a read of the DATA register. Since each interrupt sets an interrupt bit regardless of the MASK, and each interrupt bit can be selectively masked to prevent the generation of a processor interrupt, it is possible to intermix polled interrupts with true interrupts. However, polling the IR bit will cause the DATA register to clear, therefore, it is up to the user to preserve the information contained in the DATA register if any polled interrupts were present.

The MASK register provides convenient control of individual mask bits. When writing to the MASK register, if bit 7 (SET/$\overline{CLEAR}$) of the data written is a ZERO, any mask bit written with a one will be cleared, while those mask bits written with a zero will be unaffected. If bit 7 of the data written is a ONE, any mask bit written with a one will be set, while those mask bits written with a zero will be unaffected. In order for an interrupt flag to set IR and generate an Interrupt Request, the corresponding MASK bit must be set.

READ (INT DATA)

REG	NAME								
D	ICR	IR	0	0	FLG	SP	ALRM	TB	TA

WRITE (INT MASK)

REG	NAME								
D	ICR	S/$\overline{C}$	X	X	FLG	SP	ALRM	TB	TA

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